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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,090	06/14/2001	Yasunori Satoh	OKI 276	3818

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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,090	SATOH, YASUNORI	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,10-15,17 and 18* is/are allowed.

6)☒ Claim(s) *1,2,4 and 16* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1,4,16** are rejected under 35 U.S.C. 102(b) as being anticipated by Watson, U.S. Pat. No. 5,034,814.

Considering claim **1**, Watson discloses all claimed subject matter, note;

a) a delay circuit delaying the input data with a plurality of delay times so that the delay circuit outputs a plurality of delayed input data, is met by delay circuits 53 and 55, FIG.21;

b) a counter circuit that counts a pixel number of each line in the input data, is met by counter 132, FIG.21;

c) a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and outputs a calculated difference signal, is met by the Switch control 49', FIG.21; (see also col. 15, lines 11-17)

d) a selector combining the delayed input data in response to the calculated difference signal to generate as an output data combined input data having the standard

number of pixels, is met by the Switch 51, FIG.1;

Considering claim **4**, a video signal control circuit as claimed in claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal, is met by the disclosure on col. 15, 11-17.

Considering claim **16,** a video signal control circuit as claimed in Claim 1, wherein the counter circuit counts the pixel number of each line in the input data in response to a horizontal synchronous signal received by the counter circuit, is met by reset signal form the HD sync separator 47', fig.21;

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson, U.S. Pat. No. 5,034,814.

Considering claim **2**, a video signal control circuit as claimed in claim 1, wherein the delay circuit includes plural flip-flop circuits, and the plural flip-flop circuits convert the pixels constituting the input data into plural output data with each delayed by one clock.

Regarding claim 2, the Examiner takes official notice in that it is notoriously well known in the art that to construct delay circuits from a plurality of flip flop circuits, and therefore it would have been obvious to the skilled in the at the time the invention was made to modify the system of Watson by providing a plurality of flip-flop circuits in order to utilize a reliable circuit design and cut cost of the overall system as well.

Allowable Subject Matter

5. Claims **6,7,10-15, 17 and 18** are allowed.

6. Claim **5** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose, a video signal control circuit comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial delay in accordance with the inclination of the pixel dispersion, as in claim **5;**

A video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising, memory circuit which the input data can be

written in and read from, which includes two one-port memories, wherein the input data are alternately written in the two one-port memories, and the written input data are alternately read from the two one-port memories, an address generation circuit that outputs a write address or a read address to the memory circuit, a counter circuit that counts a pixel number of each line in the input data; a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and the calculated difference; an output selector combining the input data read from the memory circuit based on the new address to generate as an output data combined input data having the standard number of pixels, as in claim **6**;

A video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising: a memory circuit including a two-port memory that is able to write in and read out the input data in parallel; an address generation circuit that outputs a write address or a read address to the memory circuit; a counter circuit that counts a pixel number of each line in the input data; a judgment circuit that calculates a difference between a set standard pixel umber and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and a delay on the basis of the calculated difference; wherein the address generation circuit generates the write address signal or the read address signal on the basis of the

address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, the input data read from the memory circuit according to the plural read addresses constituting an output data of the video signal control circuit, as in claim **7**.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
December 1, 2004

PAULOS M. NATNAEL
PATENT EXAMINER